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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/00 — A1

(11) International Publication Number: **WO 97/14177**

(43) International Publication Date: 17 April 1997 (17.04.97)

(21) International Application Number: PCT/US96/16138

(22) International Filing Date: 9 October 1996 (09.10.96)

(30) Priority Data:

60/005,288	13 October 1995 (13.10.95)	US
08/727,209	8 October 1996 (08.10.96)	US

(81) Designated States: JP, KR, SG, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

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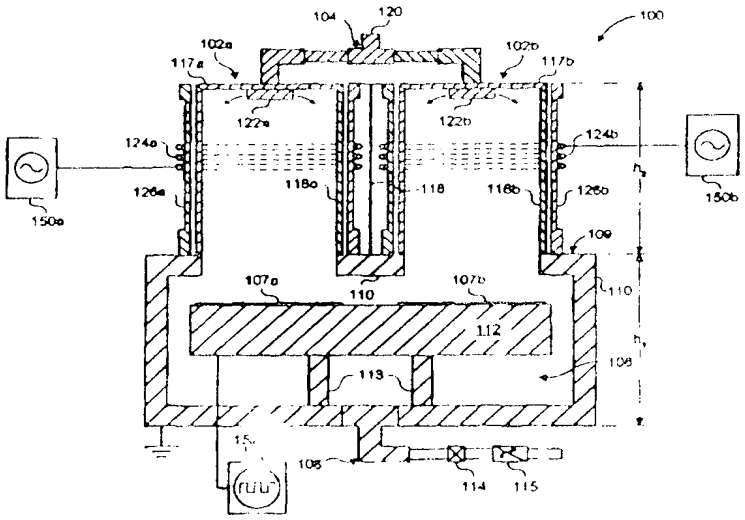
(54) Title: APPARATUS AND METHOD FOR PULSED PLASMA PROCESSING OF A SEMICONDUCTOR SUBSTRATE



(57) Abstract

Apparatus (100) for an improved etch process. A power source (1500, 1506) alternates between high and low power cycles to produce and sustain a plasma discharge. The high power cycles couple sufficient power into the plasma to produce a high density of ions ($\geq 10^{11} cm^{-3}$) for etching. The low power cycles allow electrons to cool off to reduce the average random (thermal) electron velocity in the plasma. The low power cycle is limited in duration as necessary to prevent excessive plasma loss to the walls (116a, 116b) or due to recombination of negative and positive ions. A separate power (152) source alternates between high and low power cycles to accelerate ions toward the substrate (107) being etched. In one embodiment, a strong bias is applied to the substrate in short bursts. Multiple burst occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. Ions are pulsed toward the surface for etching.

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APPARATUS AND METHOD FOR PULSED PLASMA PROCESSING OF A SEMICONDUCTOR SUBSTRATE

Background of The Invention

1. Reference to Related Application

The present application claims priority from provisional application no. 60/005,288 filed October 13, 1995. Provisional application no. 60/005,288 is hereby incorporated herein by reference in its entirety.

2. Field of the Invention

The field of the invention relates generally to semiconductor processing. More particularly, the field of the invention relates to an apparatus and method for pulsed plasma etching of a semiconductor substrate.

3. Description of the Related Art

Plasmas have been used in a variety of processes for the manufacture of integrated circuit devices including etching, stripping of photoresist and plasma enhanced chemical vapor deposition. The plasma is created by providing energy to a gas in a reactor chamber. The plasma consists of two qualitatively different regions: a quasi-neutral, equipotential conductive plasma body and a boundary layer called the plasma sheath. The plasma body comprises a plurality of mobile charge carriers and thus is a conductive medium. Its interior generally has a uniform electric potential. A plasma cannot exist for long in direct contact with material objects and rapidly separates itself from objects by forming a non-neutral sheath. The sheath is an electron deficient, poorly conductive region having a strong electric field. This electric field typically extends perpendicularly between the plasma body and any interface with material objects, such as reactor walls and wafers placed within the reactor.

Plasma reactors typically provide energy to the gas in the reactor chamber by coupling RF electric power into the chamber. The RF power coupled into the reactor chamber ionizes, dissociates, and excites molecules within the plasma body. In particular, the RF power provides energy to free electrons in the plasma body. Ionization occurs when an energized free electron collides with a gas molecule causing the gas molecule to ionize. Dissociation occurs when an energized free electron collides with a gas molecule, such as O_2, causing the molecule to break into smaller molecular or atomic fragments, such as

atomic oxygen, for example. Excitation occurs when the collision does not break molecular bonds but rather transfers energy to the molecule causing it to enter an excited state. Control of the relative amounts of ionization, dissociation, and excitation depends upon a variety of factors, including the pressure and power density of the plasma. The plasma body typically consists of radicals, stable neutral particles and substantially equal densities of negatively and positively charged particles.

Plasmas may be particularly useful for anisotropic etching of a semiconductor substrate. Anisotropic etching is etching that occurs primarily in one direction, whereas isotropic etching is etching that occurs in multiple directions. Anisotropic etching is desirable for manufacturing integrated circuit devices, because it can be used to produce integrated circuit features having precisely located sidewalls that extend substantially perpendicularly from the edges of a masking layer. This precision is important in devices that have a feature size and spacing comparable to the depth of the etch.

To accomplish an anisotropic plasma etch, a semiconductor substrate such as a wafer may be placed in a plasma reactor such that the plasma sheath forms an electric field perpendicular to the substrate surface. This electric field accelerates ions perpendicularly toward the substrate surface for etching. One conventional approach to anisotropic plasma etching uses parallel planar electrodes. Often, the lower electrode acts as a pedestal for a wafer. RF power is applied to the electrodes to produce a plasma and accelerate ions toward the wafer surface.

The crystalline silicon or thin insulating layers of some modern integrated circuit designs may be damaged by high energy ion bombardment, so it may be necessary to decrease the RF power applied to the electrodes for lower ion energy etch processes. Decreasing the RF power, however, will reduce the ion density in the plasma. Decreased ion density usually decreases the etch rate.

Inductively coupled reactors have been used to overcome this problem by using separate coupling mechanisms (and therefore separate power sources) to control the ion density and ion bombardment energy. Power is applied to an induction coil surrounding the reactor chamber to inductively couple power into the chamber to produce the plasma. The inductively coupled power accelerates electrons circumferentially within the plasma and generally does not accelerate charged particles toward the wafer which is placed below the plasma. The level of power applied to the induction coil may be adjusted to control the ion

density in the plasma. Some power from the induction coil may be capacitively coupled into the plasma, however, and may accelerate ions toward the walls and the wafer. To reduce this capacitive coupling a split Faraday shield may be placed around the reactor. See U.S patent application serial no. 07/460,707 filed January 4, 1990, which is assigned of record to the assignee of the present application and which is hereby incorporated by reference. A separate source of power may be applied to a wafer support to accelerate ions toward the wafer for etching. A relatively high level of power may be applied to the induction coil to provide a plasma with a high ion density, and a relatively low level of power may be applied to the wafer support to control the energy of ions bombarding the wafer surface. As a result, a relatively high rate of etching may be achieved with relatively low energy ion bombardment.

While low energy ion bombardment may reduce damage to sensitive layers of the integrated circuit, other problems may be encountered which interfere with the anisotropic nature of the etch. In particular, low energy ions may be deflected by charges that accumulate on the wafer or mask surface during etching.

This charge buildup may result from the relatively isotropic motion of electrons in the plasma as opposed to the anisotropic motion of the ions. The normal thermal energy of the plasma causes the electrons to have high velocities because of their low mass. These high velocity electrons collide with molecules and ions and may be deflected in a variety of directions, including toward the wafer surface. While the negative bias on the wafer tends to repel electrons, the high velocity of some electrons overcomes this negative bias. The electrons are deflected in a variety of directions and have a relatively isotropic motion. As a result, electrons deflected toward the wafer surface tend to accumulate on elevated surfaces of the wafer or mask layer, rather than penetrating to the depths of narrow wafer features (which would require a perpendicular, anisotropic motion).

Ions, on the other hand, have a large mass relative to electrons and do not have high random velocities. Rather, the bias on the wafer support accelerates ions perpendicularly toward the wafer surface. This anisotropic acceleration allows ions to penetrate to the depths of narrow wafer features more readily than electrons.

As a result, negatively charged electrons tend to accumulate on the upper surfaces of the wafer or mask layer, while positively charged ions tend to accumulate in the recessed regions of the wafer that are being etched. These accumulated charges may form small

electric fields, referred to as "micro fields," near integrated circuit features on the wafer surface. While these small electric fields may have little effect on high energy ions, they may deflect low energy ions used in low energy etch processes for small integrated circuit features. The negative charge on the substrate or mask surface tends to attract positively charged ions, while the positive charge in recessed regions tends to repel these ions. As a result, low energy ions falling into recessed regions between features may be deflected into feature sidewalls, thereby undercutting the mask layer. This undercutting can degrade the anisotropic etch process and inhibit the formation of well-defined features with vertical sidewalls.

Therefore, what is needed is an improved anisotropic etch process. Preferably such a process will allow low energy ions to be used for etching small integrated circuit features while substantially eliminating the problems associated with charge build-up on the wafer surface. Preferably such a process will enable the manufacture of small integrated circuit features with well-defined vertical sidewalls.

Summary

Aspects of the present invention provide an improved etch process. One aspect of the present invention provides a power source that alternates between high and low power cycles to produce and sustain a plasma discharge. Preferably, the high power cycles couple sufficient power into the plasma to produce a high density of ions ($\geq 10^{11} cm^{-3}$) for etching. Preferably, the low power cycles allow electrons to cool off to reduce the average random (thermal) electron velocity in the plasma. Preferably, the low power cycle is limited in duration as necessary to prevent excessive plasma loss to the walls or due to recombination of negative and positive ions. During the low power cycles the power may be off.

It is an advantage of these and other aspects of the present invention that average electron thermal velocity is reduced, so fewer electrons overcome the plasma sheath and accumulate on substrate or mask layer surfaces. As the plasma electrons cool, the sheath potential decreases which allows the plasma to move closer to the substrate surface and positive ions flow to the wafer surface which neutralizes charges that have accumulated on elevated surfaces as well as within the depths of recessed features.

Another aspect of the present invention provides a separate power source that alternates between high and low power cycles to accelerate ions toward the substrate being etched. In one embodiment, a strong bias is applied to the substrate in short bursts

Preferably, multiple burst occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. During the low power cycles, the power may be off.

When intermittent bursts are used for the bias, ions are accelerated toward the substrate in pulsed waves. Ions striking the surface cause anisotropic etching of the substrate. Most ions are pulsed near the substrate surface without reaching it. During the low power cycles, these ions coast toward the surface and those that do not collide with neutral particles continue to move substantially perpendicularly to the biased surface. During the next burst, the remaining ions in the sheath are again accelerated toward the substrate for anisotropic etching. These ions are not deflected into sidewalls as readily as ions in conventional low energy etch processes due to reduced charge buildup and the relatively low duty cycle of power used to pulse ions toward the substrate surface.

In an alternate embodiment, a lower frequency A.C. bias (100 kHz to 1 MHz) is applied to the substrate. The bias may be a continuous A.C. wave or it may alternate between high power cycles (for multiple wavelengths) and low (or zero) power cycles. Preferably, the half cycles of the A.C. waveform are at least equal to the ion transit time for ions in the sheath region. When a low frequency A.C. bias is used, negative and positive ions are alternatively accelerated toward the substrate for etching. Since the etch alternates between negative and positive ions, charge buildup on the substrate surface is avoided.

Preferably, the above aspects of the present invention are combined into a single low ion energy, anisotropic etch process with reduced charge buildup and improved feature definition.

Brief Description of the Drawings

Figure 1 illustrates a wafer processing system according to a first embodiment of the present invention;

Figure 2 is a simplified top plan view of the wafer processing system according to the first embodiment;

Figure 3 shows an exemplary power signal that may be applied to an induction coil in the wafer processing system according to the first embodiment;

Figure 4 shows an alternative power signal that may be applied to an induction coil in the wafer processing system according to the first embodiment;

Figure 5 is a schematic diagram illustrating an exemplary circuit that may be used to generate the power signal of Figure 4;

Figure 6 shows a power signal that may be used to control ion bombardment in the system according to the first embodiment;

Figure 7 shows an alternate power signal that may be used to control ion bombardment in the system according to the first embodiment; and

Figure 8 is a side view of a split Faraday shield that may be used in the system according to the first embodiment.

Detailed Description

Aspects of the present invention provide a novel apparatus and method for processing semiconductor substrates. The following description is presented to enable a person skilled in the art to make and use the invention. Descriptions of specific applications are provided only as examples. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus, the present invention is not intended to be limited to the described or illustrated embodiments, but should be accorded the widest scope consistent with the principles and features disclosed herein.

In one embodiment of the present invention, two power sources are used for anisotropic plasma etching. A first power source is used to produce a stable plasma discharge with a desired ion density. The first power source is preferably applied to an induction coil which inductively couples power into the plasma. The second power source is used to bias the substrate being etched. Preferably, the substrate is positioned below the plasma region substantially parallel to the direction of the induction electric field produced by the induction coil. The second power source may be applied to a planar electrode that acts as a support for the wafer.

In this embodiment, the inductively coupled power alternates between high and low power cycles to produce and sustain a plasma discharge. The high power cycles couple sufficient power into the plasma to produce a high density of ions for etching. The low power cycles allow electrons to cool off to reduce the average electron thermal velocity in the plasma. Typically, the low power cycle is longer than the high power cycle and the plasma exists primarily in the "after glow" state. The duration of the low power cycle is

limited, however, so electrons and ions do not recombine or fall to walls in such large numbers that the ion density is insufficient for the desired etch rate, or makes the plasma hard to reignite

The low power cycles reduce the average electron thermal velocity in the plasma, so fewer electrons overcome the plasma sheath and accumulate on substrate or mask layer surfaces As the plasma cools, the sheath potential and width decrease which causes the plasma to approach closer to the substrate surface and reduces the voltage to which electron charges accumulate on elevated (resist-covered) surfaces Thus, alternating the inductively coupled power reduces the charge buildup on substrate surfaces, as it reduces the floating potential

In one embodiment, the bias on the substrate also alternates between high and low power cycles to accelerate ions toward the substrate for anisotropic etching A strong bias is applied to the substrate in short bursts Preferably, multiple bursts occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. The amplitude of the bursts is typically greater than the amplitude of continuous RF biases used in conventional low energy etch pr ses

The alternating bias accelerates ions toward the substrate during pulses only During high power bursts, ions accelerate toward the substrate Most ions are accelerated toward the substrate surface without reaching it During the low power cycles, these ions retain their anisotropic motion and those that strike elevated surfaces help to neutralize them l ring the next burst, the remaining ions near the substrate surface are again accelerated toward the substrate for anisotropic etching These ion , whe they finally strike the surface, are not deflected into sidewalls as readily as ions in conventional low energy etch processes due to reduced charge buildup and the low duty cycle of power used to pulse ions toward the substrate surface.

In an alternate embodiment, a lower frequency A C bias (100 kHz to 1 MHz) is applied to the substrate. The bias may be a continuous A C wave or it may alternate b een high power cycles (for multiple wavelengths) and low (or zero) power cycles Preferably, the half cycles of the A.C waveform are at least equal to the ion transit time for ions in the sheath region When a low frequency A C bias is used, negative and positive ions are alternatively accel d toward the substrate for etching. Since the etch alternates between negative and positive ions, charge buildup on the substrate surface is avoided

The pulsed plasma discharge and pulsed or low frequency A.C. substrate bias combine to provide a low ion energy, anisotropic etch process with reduced charge buildup and improved feature definition.

Figure 1 illustrates a side cross-sectional view of an inductively coupled plasma reactor system 100 according to a first embodiment of the present invention. The system is used for etching semiconductor substrates such as wafers or the like to form small integrated surface features with well-defined sidewalls. In particular, the system may be used to anisotropically etch small integrated circuit features that have a width on the order of or less than the depth of the etch. The system 100 uses two cylindrical plasma generation chambers 102a and 102b side by side. Similar components are used in each of the plasma generation chambers 102a and 102b. These components are identified using the same reference numeral for each chamber, except that the suffixes "a" and "b" have been added to differentiate between components for generation chamber 102a and 102b, respectively. The elements of this embodiment may also be referred to generally by their reference numeral without any appended suffix. As shown in Figure 1, the two generation chambers use substantially duplicate elements and operate substantially independently. They do, however, share a gas supply system 104, an exhaust system 106 and a substrate processing chamber 108. The system 100 allows concurrent processing of two wafers which doubles throughput. In particular, the system 100 is configured for use in conjunction with the Aspen™ wafer handling system from Mattson Technology, Inc. Of course, it will be readily apparent that aspects of the present invention may be used in any variety of plasma processing systems including systems with single or multiple plasma generation chambers.

System 100 allows ion bombardment energies to be controlled substantially independently of the ion current density. Induction coils 124 encircle the plasma generation chambers 102. These induction coils are connected to first power sources 150. A separate electrode 112 acts as a substrate support adjacent to which semiconductor wafers 107 are placed for processing. While a single electrode 112 is used for both wafers 107a and 107b, separate electrodes may be used for each wafer. Electrode 112 is coupled to a second power source 152. The power applied to electrode 112 is used to control ion bombardment energies, while the power applied to induction coils 124 is used to control ion current density.

As described above, problems associated with charge buildup are avoided by using high and low power cycles on the induction coil 124 and the electrode 112. In an exemplary configuration, the first power source applies RF power to the induction coil 112 during high power cycles and applies no power during low power cycles. RF power at 13.56 MHz is typically used, although other frequencies may be used as well. The high power cycles typically last anywhere from 5 to 100 microseconds and the low power cycles typically last from 30 to 1000 microseconds. The duration of the high power cycles is typically less than or equal to the duration of the low power cycles. The duty cycle of the high power cycles is typically greater than or equal to 10%. The above configuration is exemplary. What is desired is a high power cycle that sustains a plasma discharge with sufficient ion density for the desired etch rate, and a low power cycle that allows electrons to cool without reducing the ion density below the level required for etching and without making it difficult to sustain the plasma discharge with the next high power cycle.

In the exemplary configuration, the second power source applies a strong negative voltage pulse to the electrode during high power cycles and applies little or no voltage during low power cycles. During the high power cycles, the second power source applies a negative bias of from 20 to 500 volts on the electrode. A single square, triangular or sinusoidal pulse may be used to provide the bias during each high power cycle. The duration and frequency of the pulses are typically selected such that several pulses occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. These pulses cause the substrate to be etched by ions which are mainly "coasting" to the surface. The duration of the pulses typically range from 1% to 10% of the average ion transit time with typical values in the range of from about 0.02 to 0.2 microseconds. The frequency of the pulses typically ranges from 500 kHz to 60 MHz. The above configuration is exemplary. What is desired is an intermittent bias on the substrate that alternates between ion acceleration cycles that accelerate ions toward the substrate for anisotropic etching and charge neutralization cycles that neutralize or remove charges that have accumulated on the substrate surface.

In an alternate embodiment, a lower frequency A.C. bias (100 kHz to 1 MHz) is applied to the substrate. The bias may be a continuous A.C. wave or it may alternate between high power cycles (for multiple wavelengths) and low (or zero) power cycles. Preferably, the half cycles of the A.C. waveform are at least equal to the ion transit time for

ions in the sheath region. When a low frequency A.C. bias is used, negative and positive ions are alternatively accelerated toward the substrate for etching. Since the etch alternates between negative and positive ions, charge buildup on the substrate surface is avoided.

The structure and operation of the substrate processing system 100 according to the first embodiment of the present invention will now be described in detail. In the present embodiment, two semiconductor substrates such as wafers 107 may be placed in a processing chamber 108 for etching. The processing chamber 108 is rectangular, and has a height, h1, of approximately 25 cm. Figure 2 shows a simplified top plan view of the reactor system according to this embodiment. Referring to Figure 2, the width 202 of the processing chamber is approximately 60 cm. The depth 204 of the processing chamber measured from the outside of processing chamber wall 110 is approximately 35 cm. The plasma generation chambers 102a and 102b are positioned above the processing chamber and have an outer diameter 206 of approximately 30 cm for 8 inch wafers (40-45 cm for 12 inch wafers). The plasma generation chambers are separated by a distance 208 of approximately 28 centimeters from center to center for 8 inch wafers.

Referring to Figure 1, the processing chamber wall 110 is grounded. The processing chamber wall 110 provides a common ground for the system and comprises a conductive material such as aluminum or the like. Within the processing chamber is a powered electrode 112 that acts as a support for wafers 107 or other substrate to be processed. This electrode 112 may also be made in part of aluminum. The electrode is supported by a ceramic support 113.

As shown in Figure 1, below ceramic support 113 is a gas exhaust system 106. The gas exhaust system 106 may be driven by a conventional fan, pump or similar device. The exhaust system 106 has a throttle valve 115 for regulating the gas flow in the exhaust system 106. A shut off valve 114 is also provided.

The top surface 109 of processing chamber 108 is approximately 3-5 cm above the surface of wafers 107. The plasma generation chambers have a height, h2, of approximately 15-25 cm and, as shown in Figure 2, have an outer diameter 206 of approximately 30-45 cm. Referring to Figure 1, the plasma generation chamber walls 116 are made of a nonconductive material such as quartz or alumina and have a thickness of approximately 4 to 6 millimeters. The plasma generation chambers are covered by lids 117. The generation chambers 102a and 102b are separated by a partition 118 comprising a thin (approximately

1/16 inch thick) sheet of aluminum The partition may be an integral part of a safety cage that encloses the generation chambers and the induction coils to prevent radiation from entering the surrounding environment For purposes of clarity, the safety cage is not shown in Figure 1

A gas supply system 104 is provided above the plasma generation chambers 102 In the center of each chamber is an input pipe 120 that provides gases (such as oxygen, SF_6, $CHFCl_2$, argon or the like) to the plasma reactor chambers The gas supply system 104 and the gas exhaust system 106 cooperate to maintain a gas flow and pressure in the generation chambers that promotes ionization given the strength of the induction electric field For a SF_6/Ar gas based process (i.e., silicon etch), pressures in the range of 5-20 millitorr are used, with 7-10 millitorr being preferred. In the first embodiment, SF_6 gas is provided to each generation chamber at between approximately 10 to 50 standard cubic centimeters per minute, with 30 standard cubic centimeters per minute being typical. In addition, about 100 to 200 standard cubic centimeters of argon are provided to each generation chamber The pressure in each chamber is maintained at less than about 30 millitorr with a pressure in the range of about 7-10 millitorr being typical. It is believed, however, that total flow rates from 50 standard cubic centimeters per minute up to 300 standard cubic centimeters per minute may be used effectively in this embodiment

The induction coils are connected to first power sources 150 through conventional impedance match networks (not shown). In the present embodiment, the induction coils 124a and 124b each have three turns The induction coils 124a and 124b may have a conductor diameter of approximately 1/4 inch, and be separated turn-to-turn by about 3/8 to 5/8 of an inch from center to center The diameter from the center of each coil on one side of a plasma generation chamber to the center of the coil on the other side of the plasma generation chamber is approximately 13 inches for 8 inch wafers (about 15 inches for 12 inch wafers). In this embodiment, the center of the middle turn of the induction coil is approximately 8 cm from the top of the plasma reactor chamber for 8 inch wafers, (about 12 cm for 12 inch wafers) and approximately 3-5 cm from the top of the processing chamber 108 This allows a plasma to be generated and substantially confined near the surface of the wafers 107. The center of this middle turn is positioned approximately 12 centimeter from the wafer surface for 8 inch wafers (about 16 cm for 12 inch wafers)

In the first embodiment, the induction coils couple energy into the plasma generation chambers 102 during high power cycles to produce a plasma. During high power cycles the induction coils produce a circumferential electric field in the plasma generation chambers that is substantially parallel to the wafer surfaces. The electric field produces a plasma in the plasma generation chambers. The density of the plasma reaches a peak in the center of an annular toroid. During low power cycles for the induction coils, the plasma sheath collapses and the plasma expands coming closer to the chamber walls and wafer surfaces.

The power applied to the induction coils 124 is pulsed with a small duty cycle to reduce charge buildup on wafer surfaces (which may include mask layers). Figure 3 shows an exemplary power signal waveform 300 that may be applied to the induction coils in the system of the first embodiment. This power signal couples sufficient power into the plasma to build up and maintain a desired ion density, while allowing free electrons a "settling" period during which they can cool. This pulsing technique produces a plasma with much lower average electron thermal energies than would be possible with a non-pulsed (e.g. a continuous RF) signal of the same amplitude. The lower average electron energies reduce the number of excess electrons that can overcome the plasma sheath voltage and accumulate thereby charging up wafer surfaces. As the plasma cools, the sheath potential decreases which allows the plasma to expand closer to the wafer surface thus better neutralizing accumulated charge.

Referring to Figure 3, the high power cycles 306 comprise a series of RF pulses. In the present embodiment, RF power at 13.56 MHz is used during the high power cycles 306, although it is believed that frequencies from 2 kHz to 40.68 MHz can be used effectively in system 100. The induction coils 124 couple power into the plasma during the high power cycles 306. The remaining portion of each period comprises a low power cycle that does not couple significant power into the plasma. Of course, a low power RF signal may be applied during the low power cycles. The low power cycle should provide no more than several times less power to the plasma than the high power cycle, preferably at least 10 to 100 times less. During low power cycles the average electron thermal velocity decreases. Preferably the high power cycles are substantially shorter than the low power cycles as reflected in the duty cycle of waveform 300. The duty cycle of waveform 300 is the period of the high frequency cycle 302 divided by the total period 304. The present embodiment has a duty cycle of about 10 percent. It is believed, however, that duty cycles ranging from

about 5 percent to 30 percent may be used effectively in the first embodiment The minimum duty cycle is limited by the energy required to maintain the plasma and depends upon a variety of parameters including the chamber pressure, amplitude of the pulses, number of turns in the induction coil, and frequency of the RF power. The RF pulses in the high power cycles 306 preferably have a magnitude of less than about 10 kilowatts. The average power provided to the plasma is less than or equal to about 2 kilowatts. In alternate configurations, the amplitude and duty cycle should be selected to provide a desired average power (which typically ranges from 200 watts to 2 kilowatts).

The duration of the low power cycle ranges from about 50 to 500 microseconds. The maximum duration is typically limited due to the power required to sustain the discharge. If some power is applied during the low power cycles, their duration may be increased. In addition, when higher amplitudes are used during the high power cycles, the duration of the low power cycles may be slightly increased. The density of the plasma typically decreases during the low power cycles with a time constant on the order of 0.1 to 1 millisecond, so the ion density typically does not decrease excessively during the low power cycles.

In an exemplary embodiment, the high power cycle duration is 100 μs and the low power cycle duration is 600 μs. During the high power cycles, a 13.56 MHz signal with a magnitude of 5 kw is applied to the induction coils 124.

Figure 4 shows an alternative power signal waveform 400 that may be applied to the induction coils 124 in system 100. As with signal 300, signal 400 uses high and low power cycles to produce a plasma in the plasma generation chamber. Rather than using multiple high frequency sinusoidal pulses during the high power cycle as in Figure 3, signal 400 uses a single pulse during each high power cycle as indicated at 402a and 402b in Figure 4. Each pulse applies a time varying current to the induction coils 124 which inductively couples power into the plasma. As shown in Figure 4, both positive pulses 402a and negative pulses 402b may be used. The amplitude, frequency and duration of the pulses may be varied to achieve desired plasma properties. The amplitude of each pulse typically ranges from 1 kV to 20 kV, the frequency typically ranges from 1 kHz to 10 kHz, and the duration of the pulses typically ranges from 50 μs to 500 μs. The duty cycle is determined by dividing the duration of the high power cycle (indicated at 404a) by the total period (indicated at 406a). The duty cycle of the high power cycle typically ranges from 5% to 30%. In the system of

the second embodiment, the pulses preferably have an amplitude of about 5 kw, a frequency of 2 kHz, and a duration of 70 μs. This provides a duty cycle of 14%. During the remaining portion of period 406, no power (or low power) is coupled into the plasma.

Figure 5 is a schematic of an exemplary of circuit 500 that may be used to generate signal 400. Referring to Figure 5, signal 400 is generated by feeding a square wave from a conventional switching power supply 150 through a blocking capacitor 502. Signal 400 is applied to the induction coils 124 at node V_{400}.

The rise time of pulse 402a and the fall time of pulse 402b are determined by the amplitude of the square wave and the inductance and resistance of the induction coils 124 (which determine the RL time constant). The fall time of pulse 402a and the rise time of pulse 402b are determined by the amplitude of the square wave and the capacitance of blocking capacitor 502 and resistance of the induction coils 124 (which determine the RC time constant). The rise and fall times of the pulses determine the overall duration of the high power cycle. As will be readily apparent to one of ordinary skill in the art, the amplitude and frequency of the square wave determine the amplitude and frequency of the pulses.

While two exemplary power signal waveforms 300 and 400 have been described, any number of signals may be used in conjunction with embodiments of the present invention. What is desired is a high power cycle that sustains a plasma discharge with sufficient ion density for the desired etch rate, and a low power cycle that allows electrons to cool without reducing the ion density below the level desired for etching.

Using pulsed power to generate the plasma in the first embodiment helps decrease problems associated with charge buildup. The low power cycles allow electrons to cool, so fewer electrons are initially able to overcome the sheath potential and accumulate causing charge up on wafer surface. In addition, the sheath potential decreases during the low power cycles which allows the plasma to expand close to the wafer surface. The sheath potential is typically 3 to 5 times the plasma electron temperature divided by the charge of an electron. During low power cycles, the sheath potential may decrease to much less than a volt. The smaller sheath potential decreases the thickness of the sheath and reduces electric fields near the wafer allowing electrons closer to the wafer surface. As a result, the plasma is better able to neutralize charge that accumulates in various parts of the wafer surface.

Despite the low frequency power cycles, the system of the first embodiment achieves commercially viable etch rates. While the average power applied to the plasma is about one to two kilowatts, during high power cycles about 5-20 kilowatts may be applied to the plasma. During the high power cycles, a sufficient number of ions are generated for acceptable etch rates. The low power cycles are preferably not too much greater than the electron/ion, or negative ion-positive ion recombination time constant, so the ion density is not excessively reduced during these cycles. The low power cycles may also facilitate the formation of negative ions. During the low power cycles, electrons reach lower energy levels. At low thermal energy, electrons may combine with neutral atoms or molecules to form negative ions. As will be described below, these negative ions may be used in some embodiments to reduce charge buildup or etch the substrate.

When high frequency power is applied to the induction coil (as described above with reference to Figure 3), significant power may be capacitively coupled into the plasma in addition to the inductively coupled plasma. See U.S. patent application serial no. 07/460,707 filed January 4, 1990, which is hereby incorporated by reference. See also U.S patent application serial no. 08/340,696 filed November 15, 1994, which is hereby incorporated by reference. The capacitively coupled power modulates the plasma potential relative to the wafers. At the power levels used to produce a dense plasma, the plasma modulation may cause higher energy ion bombardment and degrade the process or damage some exposed layers on the wafer. As shown in Figure 1, a split Faraday shield 126 may be interposed between the induction coil and the plasma to reduce capacitive coupling between the coil and the plasma. Figure 8 illustrates the structure of the split Faraday shield 126 that is used in the first embodiment when high frequency power is applied to the induction coils 124. The shield 126 has vertical slots 128 that start approximately near the top of the plasma generation chambers 102 and end near the top of the processing chamber 108. This allows the shield 126 to be an integral part which simply fits over the plasma reactor chamber. The bottom of the shield 126 may be connected to the top of the processing chamber to provide a common ground for the shield 126.

In the first embodiment, the split Faraday shield is designed to allow some modulation of the plasma potential. This design makes it easier to ignite and maintain a plasma reaction in the plasma generation chambers. Nevertheless, the split Faraday shield blocks substantial capacitive coupling and limits modulation of the plasma potential to a

desired amount (order of magnitude <10 volts). The number and width of slots in the split Faraday shield may be selected to control the level of capacitive coupling and modulation. The slots 128 in the shield 126 are typically about 3/16 to 3/8 wide. The induction coil 124 surrounds the split Faraday shield around the middle portion 131 of the slots. For the split Faraday shield of the first embodiment, there are 8 slots with adjacent slots being separated by a distance of about 8.4 cm from center to center.

A second power source 152 is coupled to electrode 112 to accelerate ions toward wafers 107 for anisotropic etching. The power applied to the electrode alternates between high and low power cycles. Figure 6 shows an exemplary power signal waveform 600 that may be applied to the electrode in the first embodiment. A strong negative bias is applied to the substrate in short pulses 601. Preferably, multiple pulses occur during the average transit time for an ion to cross the plasma sheath and reach the wafer surface. A typical ion transit time is estimated to be about 1 microsecond, and the pulse duration 604 in the first embodiment typically ranges from about 0.03 to 0.3 microseconds. In the first embodiment, the pulses 601 have a frequency in the range of about 1 to 5 MHz. Alternative embodiments may use frequencies ranging from about 500 kHz to 20 MHz.

Each pulse 601 is followed by a low power cycle during which a low voltage of opposite sign bias is applied to the electrode such that the time average voltage is nearly zero. In the first embodiment, the duty cycle of the pulses, as determined by the pulse duration 604 divided by the total period 606 (i.e., the combined duration of a high and low power cycle), is typically in the range of about 10 to 20 percent. Alternative embodiments may use duty cycles ranging from about 5 percent to 50 percent. The duty cycle that is used with a particular embodiment will depend on a number of factors, including the desired etch characteristics (rate, sidewall profile, selectivity), the acceptable ion bombardment energies, the amplitude of the pulses, and other plasma characteristics such as density and plasma potential.

Signal 600 has a DC offset 602 on the order of one to two tenths of the absolute value of the amplitude of the negative pulses 601. The amplitude 608 of the pulses 601 is preferably in the range of about negative 100 to negative 300 volts. Alternate embodiments may use pulses having amplitudes in the range of from about negative 10 volts to negative several thousand volts. The average ion bombardment energy in the present embodiment, with three to five megapulses per second, 10 percent duty cycle, and an amplitude between -

100 and -200 volts is about 10 to 20 electron volts. This average ion bombardment energy (in combination with the low electron temperature and plasma potential) provides a low ion energy etch even though the pulses have large amplitudes

The alternating bias accelerates ions toward the wafers in pulsed waves. During the high power negative pulses, positive ions accelerate toward the wafers. Some ions are pulsed near the wafer surface without reaching it. During the low power cycles, these ions drift at constant velocity. Some may exchange charge with other particles or make large angle collisions. Ions flowing to the surface help neutralize any negative charge that has accumulated on elevated wafer surfaces. During the next pulse, the remaining ions near the wafer surface are accelerated toward the wafer for anisotropic etching. These ions are not deflected into sidewalls as readily as ions in conventional low energy etch processes due to reduced charge buildup, the relatively low duty cycle of the pulses used to accelerate ions toward the wafer, and the low plasma potential.

The low power cycles may also reduce charge buildup by reducing the electron kinetic energy and hence the accumulated charge on exposed surfaces. In particular, the plasma can charge up the wafer surface to a voltage proportional to the electron temperature during periods when the inductively coupled power is in its low power cycle.

A variety of alternative signals may be used to provide a pulsed bias on electrode 112. For instance, a slightly positive DC bias of several volts may be used during the low bias power cycles to attract negative charge to neutralize the positive charge that has accumulated in the depths of recessed wafer features. Alternatively, a short low power positive pulse 610 may be applied to the electrode after each high power negative pulse. The positive pulses would last for only a small portion of the low power cycle to attract negative charge which builds up on recessed features of the wafer. Any positive charges would also be briefly repelled with minimal effect on ion motion. During the unbiased portion of the low power cycle, any remaining charge would be neutralized. An amplitude of less than about 10 volts and a duration about equal to the duration of pulses 601 may be used for these positive pulses in the first embodiment.

In the first embodiment, the power from the second power source is applied to the electrode 112 using a very low inductance and stray capacitance conductor. This low impedance connection causes signal pulses to be undiminished by the transmission between

the electrode 112 and source. This low impedance connection may be important to ensure that the signal pulses produce the desired bias on the electrode.

An alternate embodiment may be configured to use negative ions as well as positive ions for etching. Negative ions tend to be formed when electrons in the plasma have low average energies. The electrons tend to recombine with neutral atoms and molecules which are more abundant in the plasma than positive ions. A low (or zero) power should be applied to the induction coils during the low power part of the cycle to promote the formation of negative ions. Positive and negative ions may be used for etching by applying both negative and positive biases to the wafer. If the plasma potential is too high, however, the negative ion density will be too low to contribute significantly to etching.

When the inductively coupled power is adjusted to produce a plasma with a large number of negative ions, a lower frequency sinusoidal power signal may be applied to electrode 112 to alternatively accelerate positive and negative ions toward the wafer surface. Figure 7 shows an exemplary signal 700. As shown in Figure 7, signal 700 has both positive and negative portions relative to DC offset 701 (which is preferably zero). Positive ions will be accelerated toward the wafer during portions of the signal having a negative voltage, and negative ions will be accelerated toward the wafer during portions of the signal having a positive voltage. Thus, both positive and negative ions may be used for etching. Signal 700 has a frequency of about 50 kHz to 1 MHz, although other frequencies may be used as well. The signal does not have to be symmetric about DC offset 701. It may be desirable to have a longer negative bias with a larger amplitude if there are more positive ions available for etching. A self-bias develops in this case. In addition, the negative and positive pulses may be separated by a period having no bias to allow charge to neutralize on the wafer surface. Alternatively, a square or triangular power signal waveform with both negative and positive portions may be used to accelerate positive and negative ions for etching.

While this invention has been described and illustrated with reference to particular embodiments, it will be readily apparent to those skilled in the art that the scope of the present invention is not limited to the disclosed embodiments but, on the contrary, is intended to cover numerous other modifications and equivalent arrangements which are included within the spirit and scope of the following claims.

Claims

What is claimed is:

1. A plasma reactor for anisotropically etching a semiconductor substrate comprising:

a reactor chamber for producing a plasma;

an induction coil surrounding at least a portion of the reactor chamber;

a first power source coupled to the induction coil such that the induction coil couples power into the plasma using both high power cycles and low power cycles;

the substrate being positioned adjacent to the plasma; and

a second power source applying an intermittent bias to the substrate to accelerate ions toward the wafer for etching.

2 The plasma reactor of claim 1 wherein the plasma has a potential and an ion density, the potential of the plasma is substantially larger during the high power cycles than during the low power cycles, and the ion density of the plasma during the high power cycles is within an order of magnitude of the ion density of the plasma during the low power cycles.

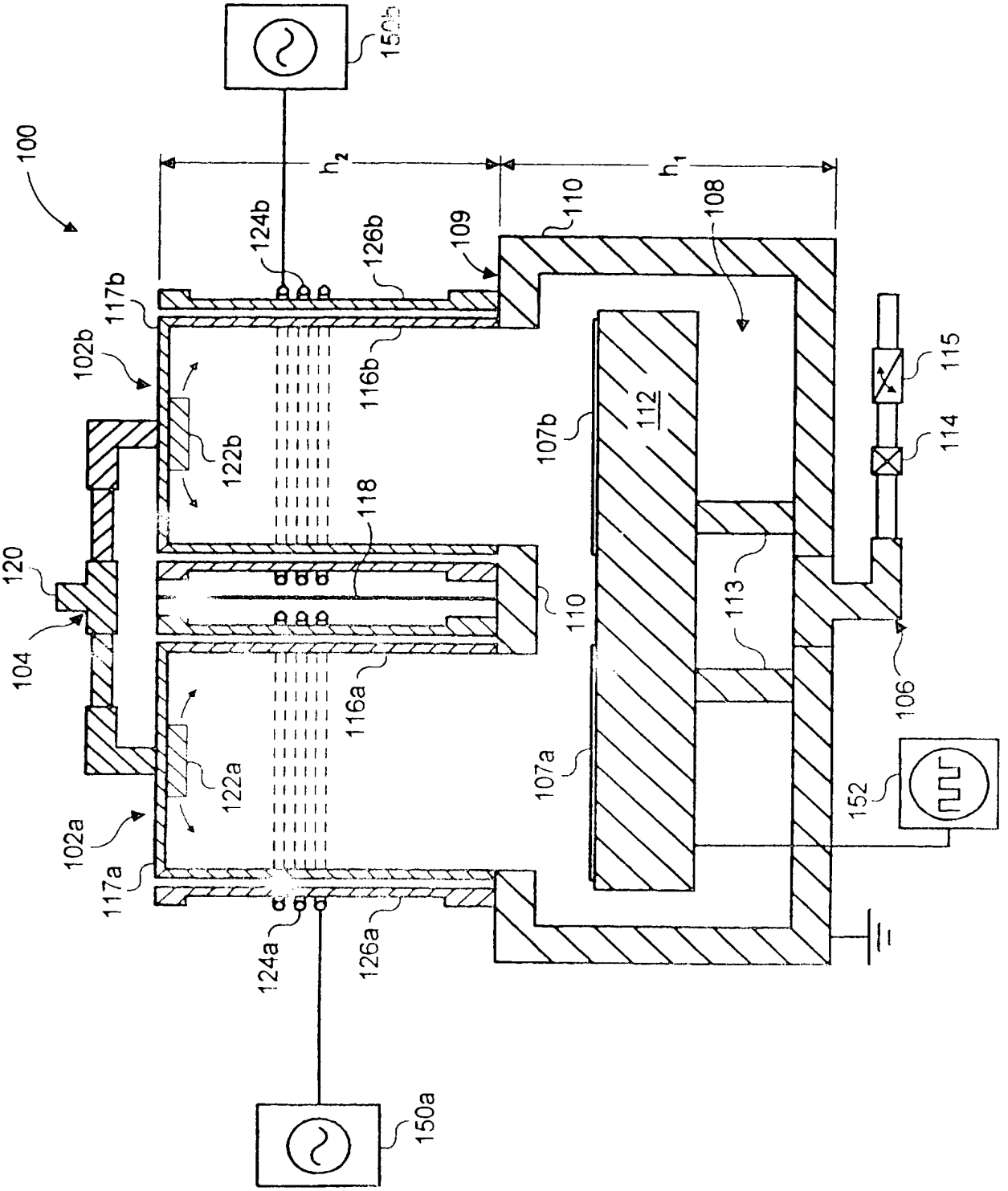

Figure 1

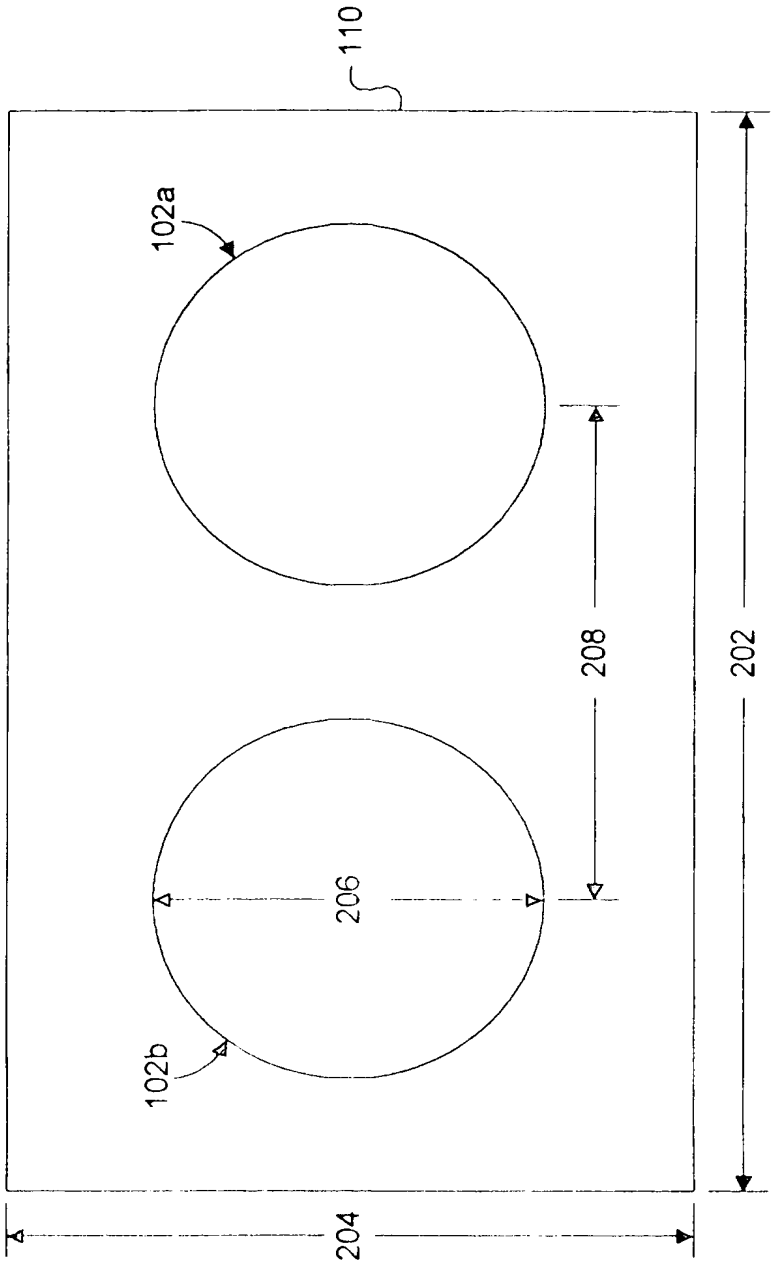

Figure 2

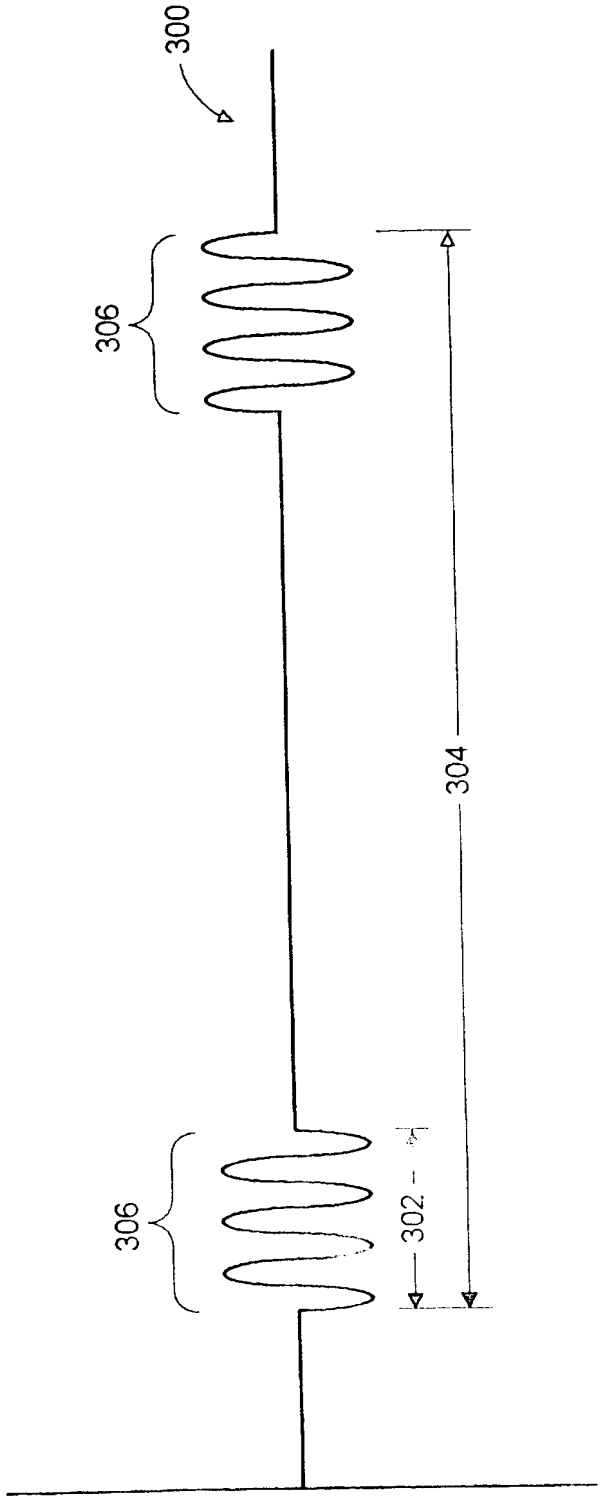

Figure 3

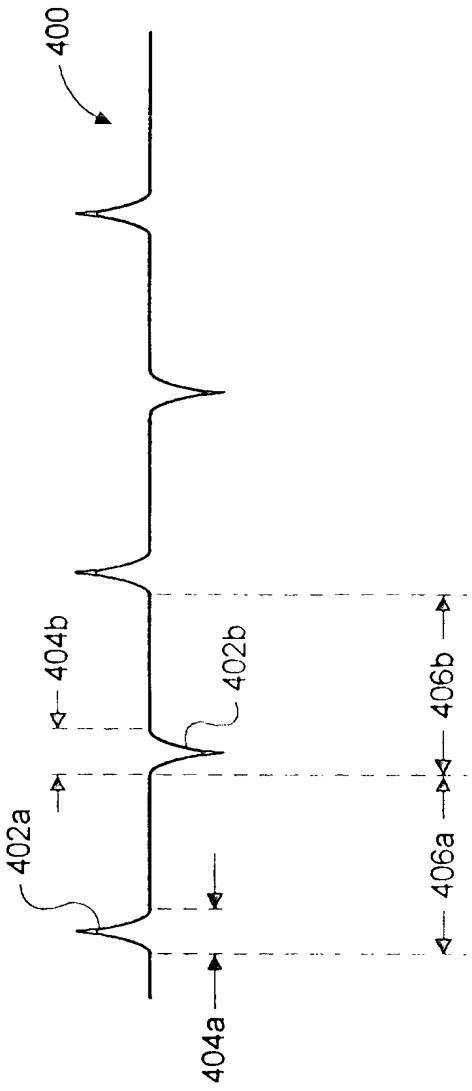

Figure 4

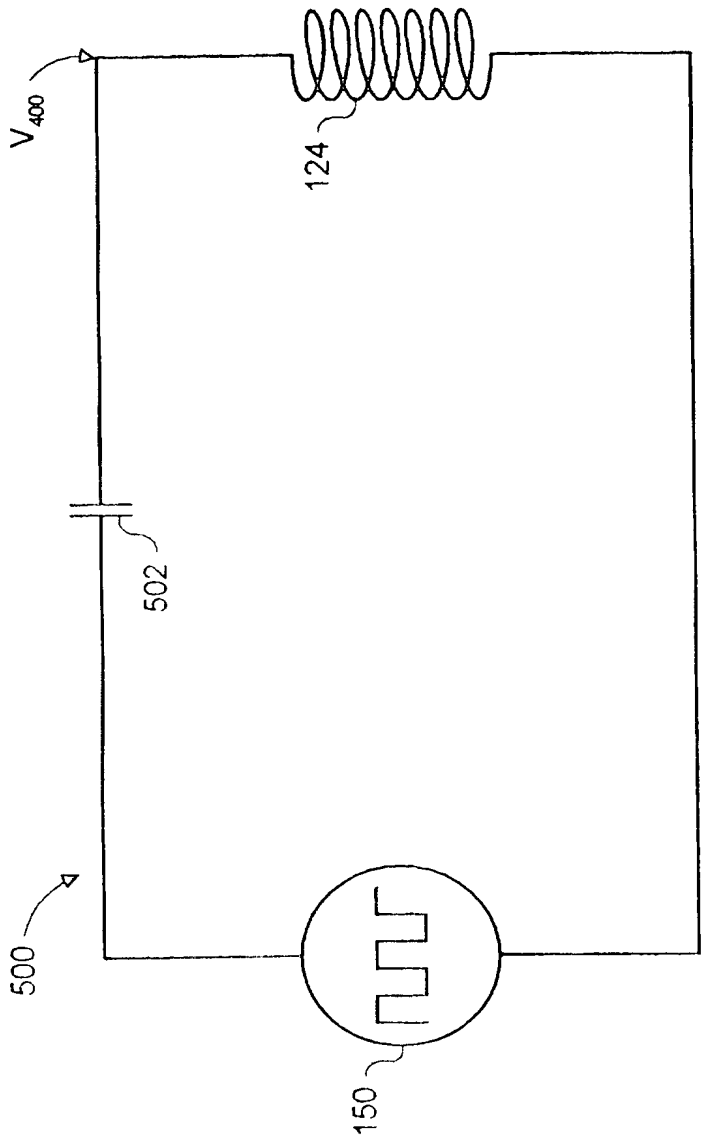

Figure 5

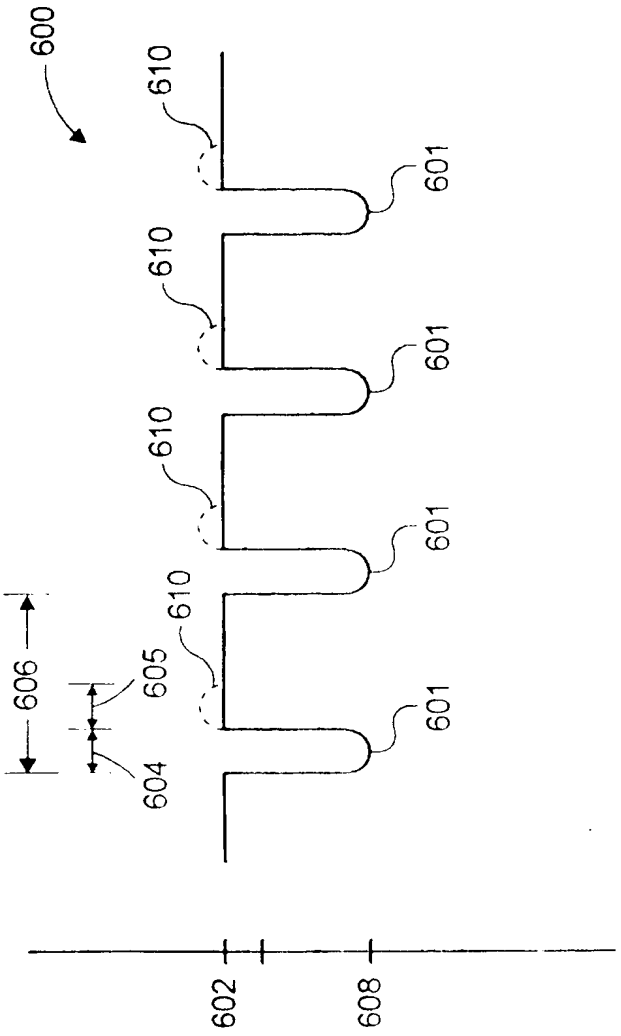

Figure 5

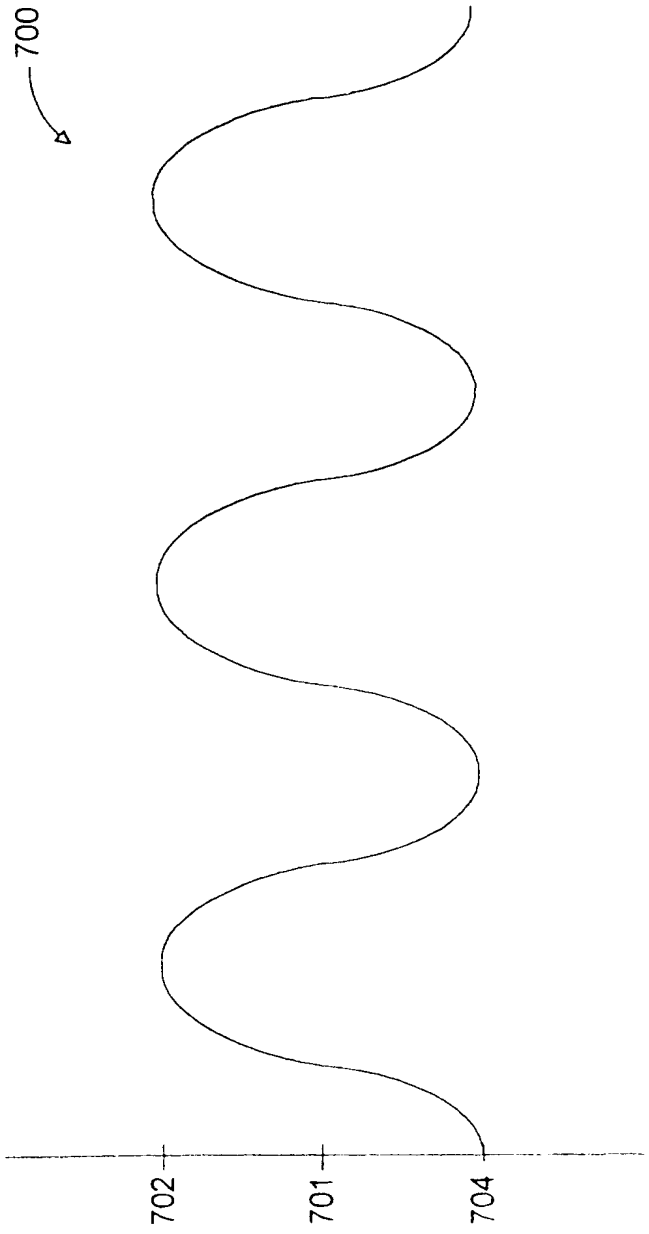

Figure 7

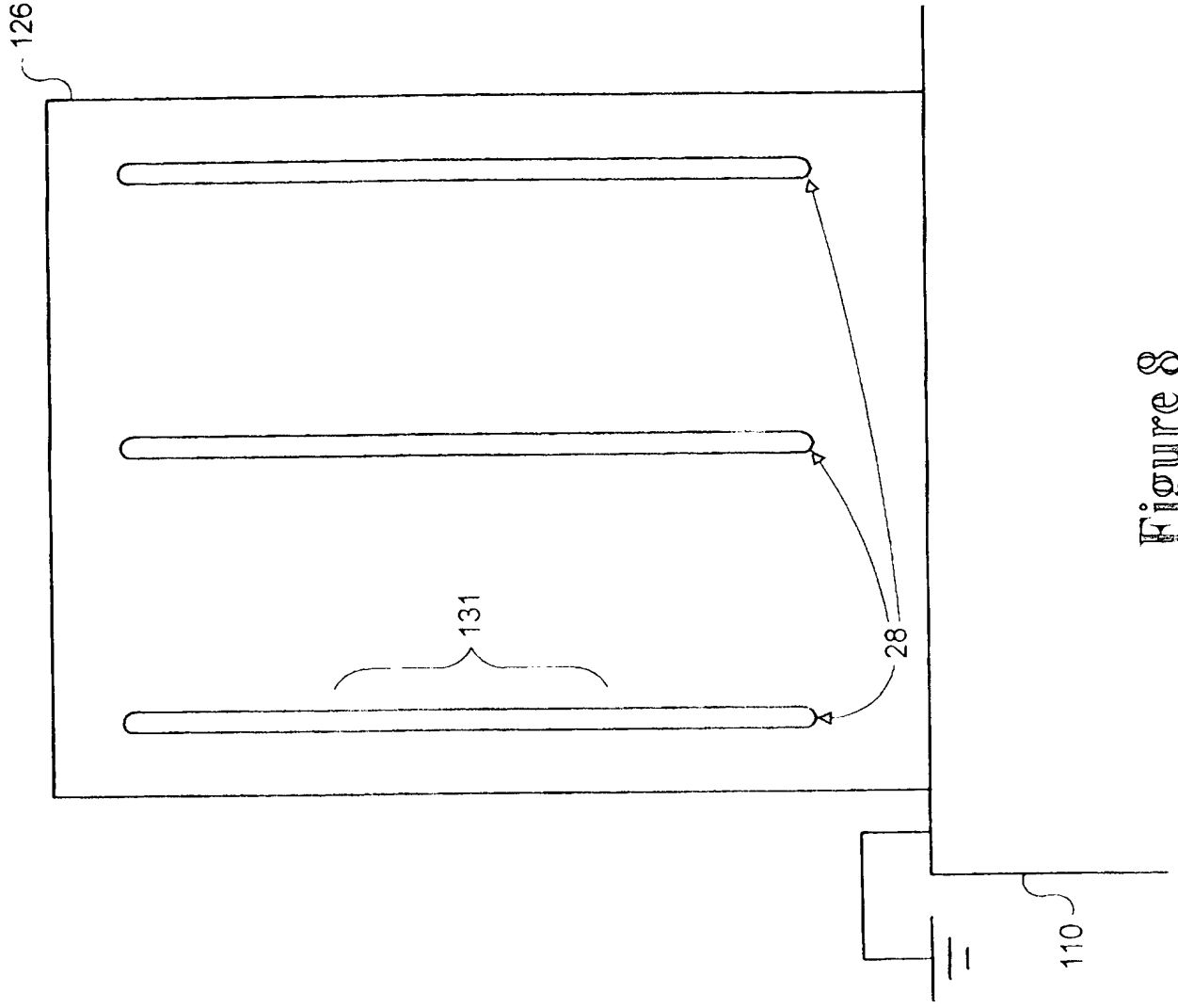

Figure 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/16138

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 21/00
US CL : 156/345
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 156/345,643.1;204/2.98.34,298.38;216/67

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,500,563 A (ELLENBERGER ET AL) 19 February 1985 (19/02/85), see entire document.	1-2
A,P	US 5,556,501 A (COLLINS ET AL) 17 September 1996 (17/09/96), see entire document.	1-2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 21 FEBRUARY 1997	Date of mailing of the international search report 07 MAR 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer WILLIAM A. POWELL Telephone No. (703) 308-1975

Form PCT/ISA/210 (second sheet)(July 1992)*

US005880034A

United States Patent [19]

Keller

[11] Patent Number: 5,880,034

[45] Date of Patent: Mar. 9, 1999

[54] **REDUCTION OF SEMICONDUCTOR STRUCTURE DAMAGE DURING REACTIVE ION ETCHING**

[75] Inventor: **John H. Keller**, Newburgh, N.Y.

[73] Assignee: **Princeton University**, Princeton, N.J.

[21] Appl. No.: **841,218**

[22] Filed: **Apr. 29, 1997**

[51] **Int. Cl.**[6] **H01L 21/00**

[52] **U.S. Cl.** **438/732**; 156/345; 216/70

[58] **Field of Search** ..... 156/345 ME, 345 MG; 216/67, 70; 438/732, 728; 204/298.37, 298.38

[56] **References Cited**

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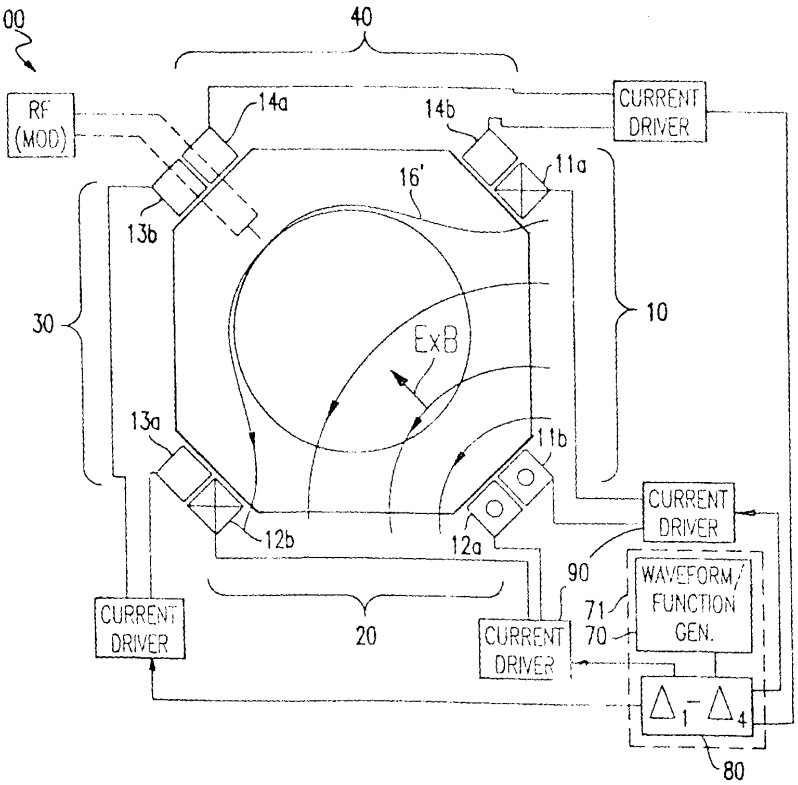
Primary Examiner—William Powell

Attorney, Agent, or Firm—Glenn E. Karta

[57] **ABSTRACT**

Uniformity of plasma density and potential are increased by reducing plasma confinement through use of a non-uniform, graded magnetic field by asymmetric energization of electromagnets with a waveform including harmonics of a fundamental frequency. The magnetic field strength or intensity decreases in the direction of ExB drift of energetic electrons within the plasma which tends to cause additional ionization in the plasma and a gradient of plasma density and potential. Thus, increase in ionization due to ExB drift is balanced by reduction of plasma confinement. Uniformity of average exposure to the plasma is further increased by rotation of the magnetic field. Uniformity of plasma potential or wafer bias is further improved by modulation of the radio frequency (RF) power used to form the plasma in synchronism with decreases in the magnetic field during switching for magnetic field rotation.

18 Claims, 4 Drawing Sheets



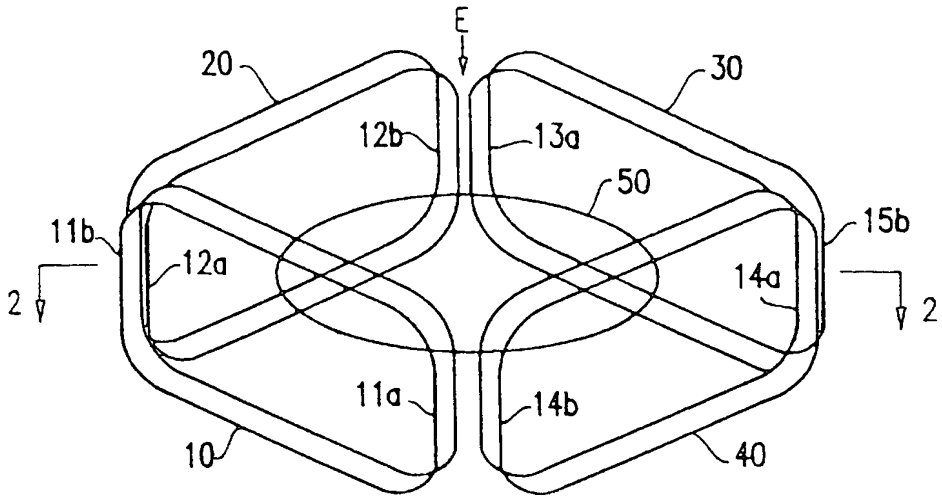


FIG.1

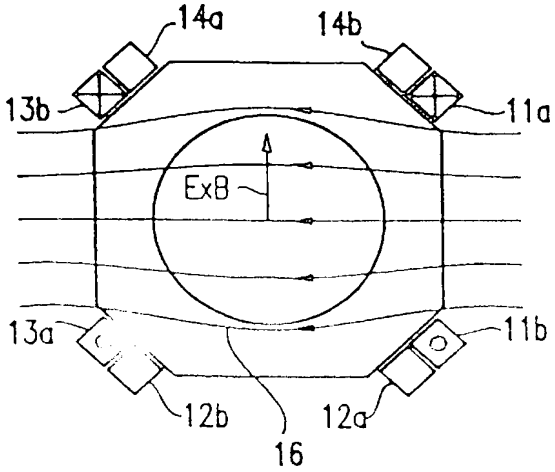


FIG.2A
RELATED ART

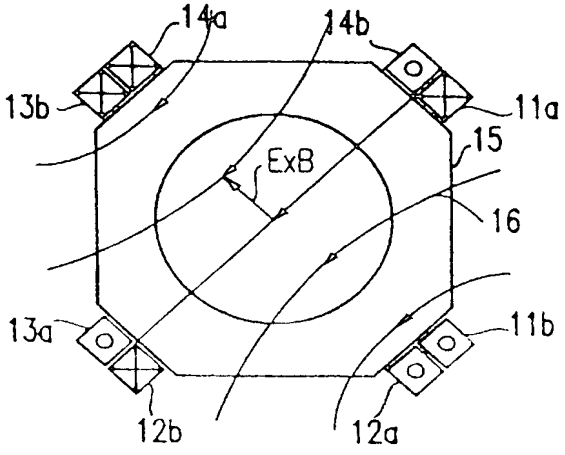


FIG.2B
RELATED ART

FIG.2C

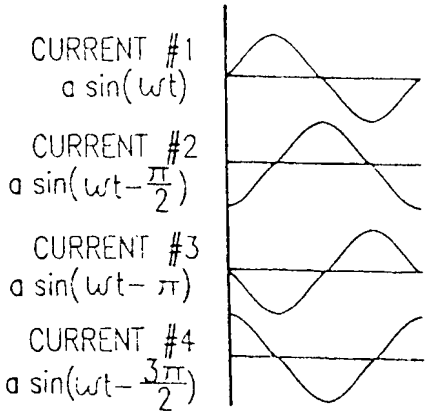
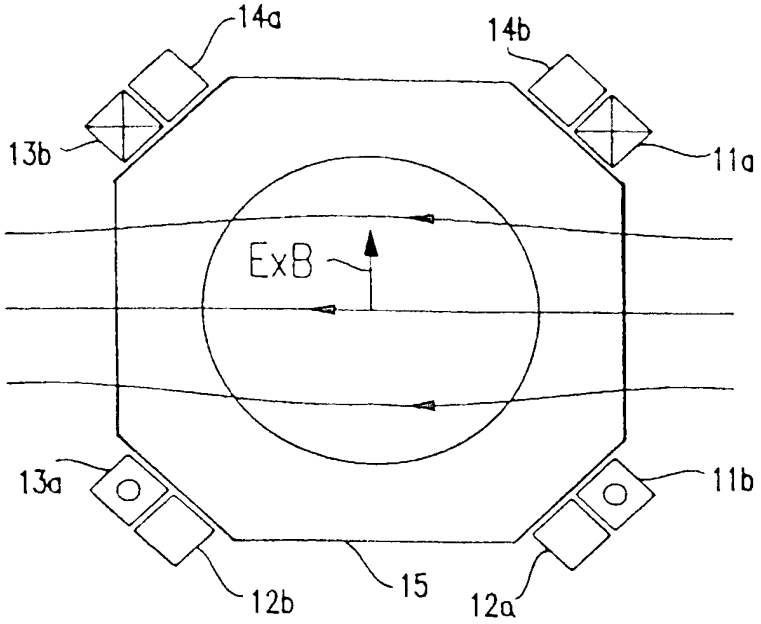


FIG.3A



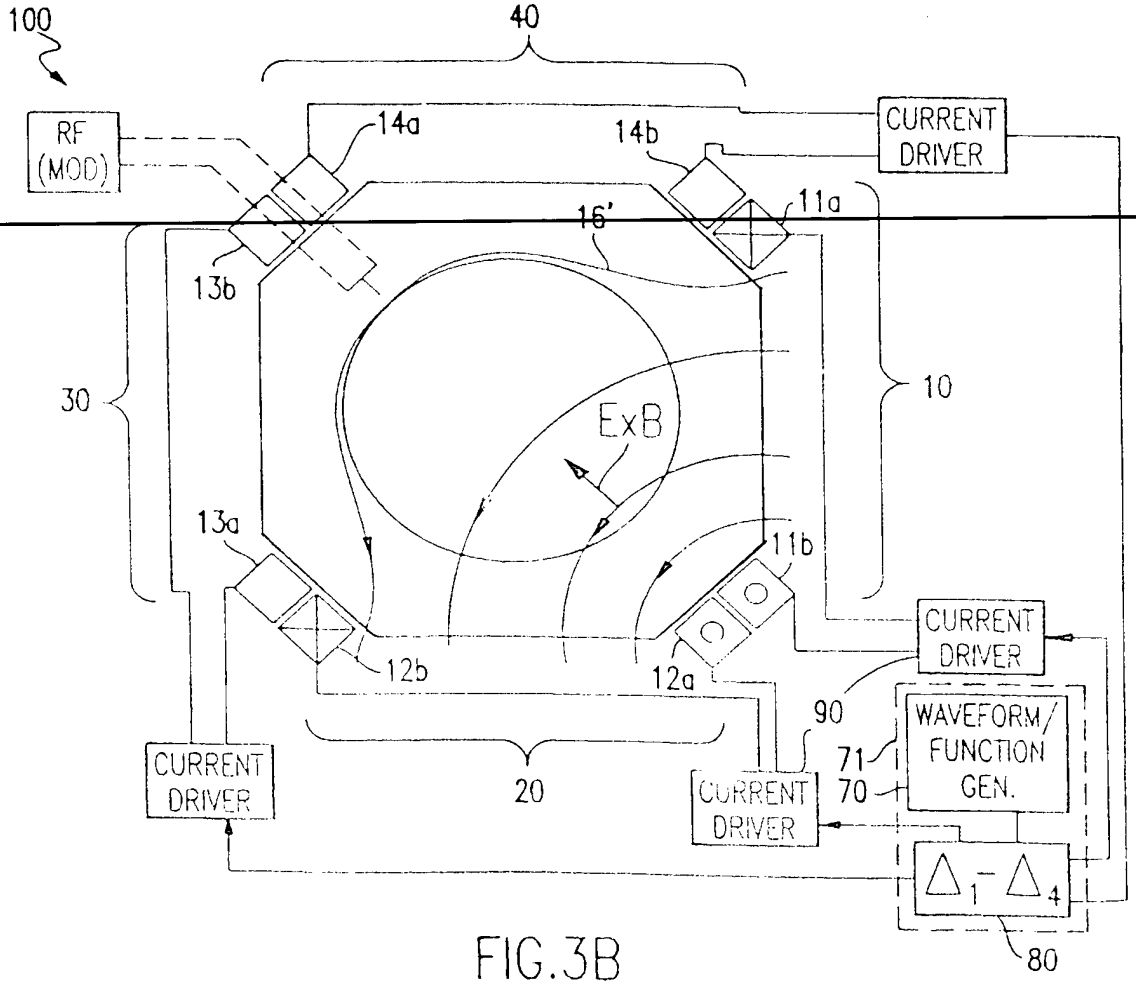


FIG.3B

CURRENT #1, COIL 10
$I_1 = F(t)$

CURRENT #2, COIL 20
$I_2 = F(t-\frac{\pi}{2})$

CURRENT #3, COIL 30
$I_3 = F(t-\pi)$

CURRENT #4, COIL 40
$I_4 = F(t-\frac{3\pi}{2})$

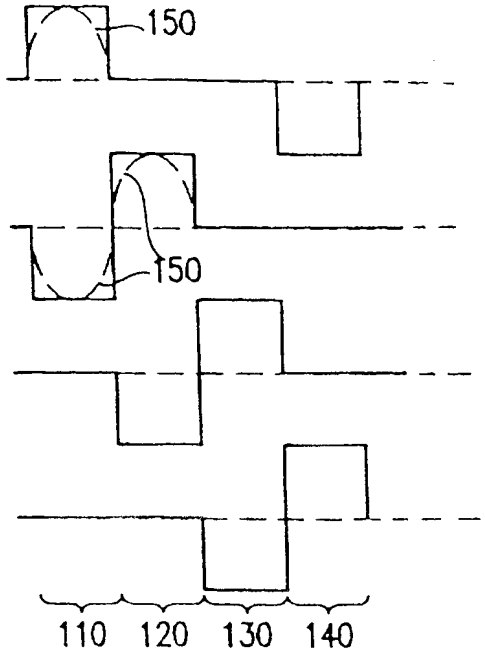


FIG.4A

CURRENT #1
$I_1 = G(t)$

CURRENT #2
$I_2 = G(t-\frac{\pi}{2})$

CURRENT #3
$I_3 = G(t-\pi)$

CURRENT #4
$I_4 = G(t-\frac{3\pi}{2})$

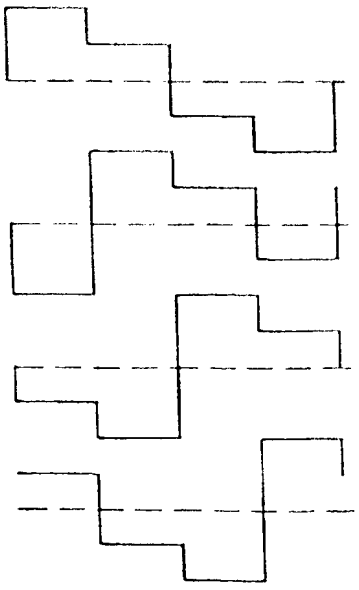


FIG.4B

FIG.4C

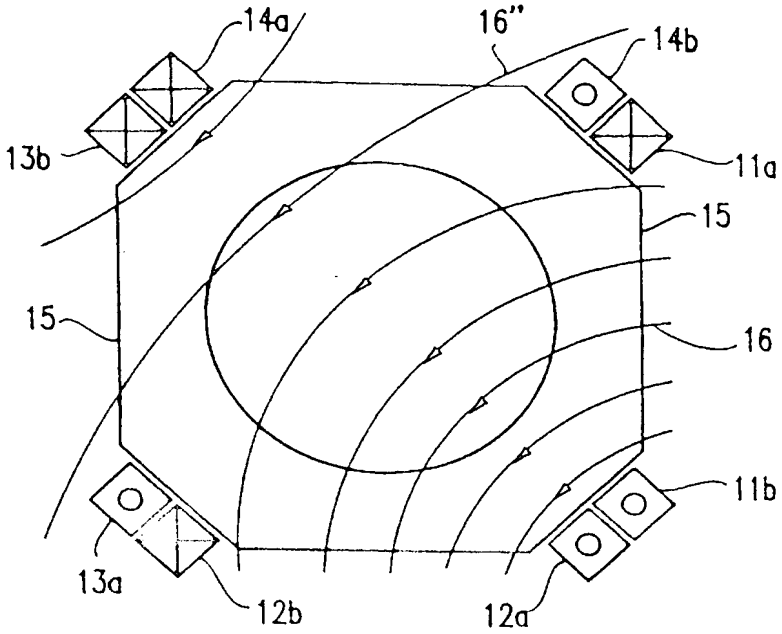


FIG.5A

FIG.5B

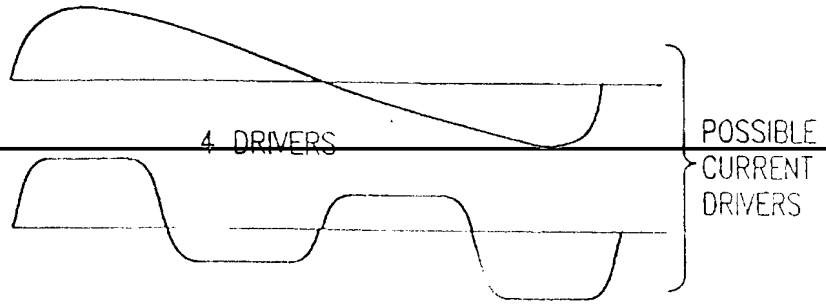
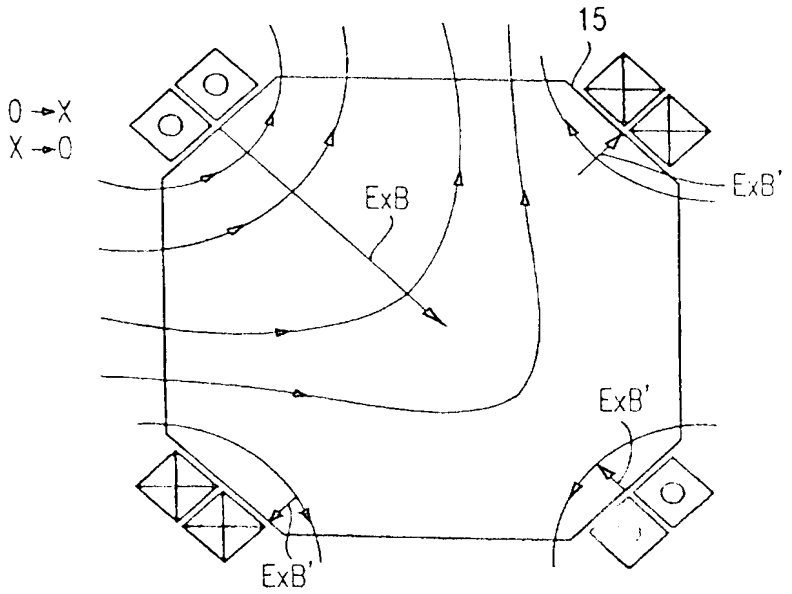


FIG.6



REDUCTION OF SEMICONDUCTOR STRUCTURE DAMAGE DURING REACTIVE ION ETCHING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to the manufacture of semiconductor devices and, more particularly, to the performance of reactive ion etching and the reduction of damage to semiconductor wafers and earlier formed structures during reactive ion etching.

2. Description of the Prior Art

Scaling of electronic element structures to smaller sizes in semiconductor integrated circuits having increased integration density (to obtain improvements in propagation speed, noise immunity and economy of manufacture) has increased the criticality of many wafer processing operations. At the same time, there has also been a trend to increase wafer size to permit process costs to be spread over an increasing number of chips which may compromise the accuracy with which processing can be performed. For example, reactive ion etching is generally considered to be a relatively rapid, well-controlled process useful at numerous stages of integrated circuit manufacture but has presented criticality which has compromised manufacturing yields in modern integrated circuit designs.

During reactive ion etching, a plasma generated by radio frequency (RF) electric field energy and confined by a magnetic field (to increase plasma density and allow reduction of RF energy and bias) is used to develop charged species (electrons and ions). An etchant is introduced into the chamber **15** and ionized and the ions are accelerated toward a wafer by an electric field to etch the surface thereof in a manner well-understood in the art. The speed of the etching process and throughput of the apparatus in which it is conducted is dependent on the density of the plasma adjacent a particular region of the wafer and it is generally desirable to form a plasma with a high density of charged species. By the same token, however, the density of plasma to which the wafer is exposed must, at least on average, be substantially uniform to achieve the same etch rate at all points on the wafer surface particularly for very large diameter wafers.

Reactors for the performance of reactive ion etching must accommodate at least one wafer and thus are of sufficient size to allow local variations and non-uniformity in density of the plasma. Therefore, it has become the practice to use a rotating magnetic field above the wafer to cause the plasma to be repeatedly swept across the surface of the wafer to increase uniformity of exposure of the wafer to the plasma even when the plasma density is not uniform.

However, both increase in size of reactor chambers to accommodate larger wafers and increases in process criticality as electronic elements are scaled to smaller sizes has resulted in damage to wafers due to plasma non-uniformity becoming a significant factor in manufacturing yield. At larger reactor or wafer sizes, a magnetron effect causes a gradient of plasma density across the wafer. The gradient of plasma density, in turn, produces a variation of plasma potential across the wafer because of the tendency of energetic electrons from the plasma to drift in a direction perpendicular to both the magnetic field and the electrical field, referred to as the ExB drift. This drift of electrons causes additional ionization which produces further energetic electrons to contribute to the electron drift and further contribute to the gradient of plasma density across the wafer.

It can be understood that this effect will increase for larger reactor and wafer sizes and can become great enough to damage thin gate oxide films in FET arrays and other structures which become very thin when scaled to smaller sizes for higher integration density.

On the other hand, if no magnetic field is used to increase plasma density, an increased bias voltage of about 1 KV or higher is necessary to maintain a sufficient density of plasma above the wafer for reactive ion etching to proceed at an acceptable rate. However, this large bias voltage is sufficient to cause X-ray damage to oxides and lattice damage to the wafer. Therefore, it is the practice to use both a magnetic field and reduced electric field bias for reactive ion etching. However, the ExB drift (and its effect on non-uniform plasma density) is, of course, a function of both electrical and magnetic field strength or intensity and the plasma density developed, which, for a given reactor or wafer size, effectively places a limitation on the magnitude of both the electrical bias and magnetic field which can be used, limiting throughput of the reactor.

An article entitled "Reduction of Charge-up Damage in Magnetron RIE" by Yukimasa Yoshida, published in Electrochemical Society Proceedings, Vol 95-5, pages 236–245, reports that uniform magnetic fields near the wafer surface cause damage and that damage can be reduced by using a non-uniform magnetic field in a magnetron RIE reactor using a rotating plurality of permanent magnets to obtain increased uniformity of plasma density and plasma potential. However, permanent magnets do not allow the magnetic field to be varied to optimize the plasma density or magnetic field gradient in accordance with desired manufacturing process parameters and require substantial mechanical support and mechanisms to rotate them and, hence, are impractical for integrated circuit production. On the contrary, RIE reactors which have become standard in the industry generate rotating magnetic fields by applying varying currents to stationary coils in a sequence to provide a rotating magnetic field. Such arrangement do not readily lend themselves to the simultaneous production of a rotating magnetic field which is also non-uniform since any variation of coil geometry which would create magnetic field non-uniformity would be superposed with other non-uniformities from other coils as the magnetic field was rotated. That is, the gradient in magnetic field strength which might be developed for one coil would not be maintained for a plurality of coils energized by currents of differing phase to obtain field rotation. Further, since the coils currently existing in current commercial reactors constitute an expensive component thereof, alteration of coil geometry is not economically feasible to obtain a suitable non uniformity of a magnetic field which must also rotate.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a rotating non-uniform magnetic field in which the magnetic field is reduced in the direction of ExB drift in a reactor for reactive ion etching processes.

It is another object of the invention to provide reduction of charge-up damage, X-ray damage and wafer lattice damage during reactive ion etching, particularly in large reactors or for large wafers.

It is a further object of the invention to reduce throughput limitations imposed by magnetic and electric field strength and resultant gradients in plasma density and plasma potential due to ExB electron drift.

It is another further object of the invention to provide for increase of RF wafer electrode power without causing increase of plasma density or non-uniformity above the wafer.

It is yet another object of the invention to provide increased plasma density and uniformity at a given RF power and bias.

In order to accomplish these and other objects of the invention, a method of manufacturing is provided including the steps of forming a plasma including electrons and charged species, applying an electric field across the plasma, and confining the plasma with a variable magnetic field having a gradient of field strength which decreases in the direction of drift of electrons in response to the electric field and magnetic field developed in response to currents in a plurality of coils.

In accordance with another aspect of the invention, an apparatus is provided for plasma processing of a material including a source of RF power to produce a plasma, at least three electromagnets including respective current drivers therefor, a function generator for producing a waveform including a fundamental frequency and at least one harmonic of the fundamental frequency, and an arrangement for providing the waveform to respective ones of the current drivers at respective times to produce a rotating magnetic field which is asymmetric and decreasing in intensity in the direction of ExB drift of electrons in the plasma.

In accordance with a further aspect of the invention, a method of operating a plasma processing device having a plurality of electromagnets and a source of RF power to provide a plasma is provided including the steps of energizing the plurality of electromagnets asymmetrically to produce a magnetic field having a gradient of magnetic field intensity decreasing in a direction of ExB electron drift with a waveform including a fundamental frequency and at least one harmonic of the fundamental frequency, and adjusting relative magnitude of the harmonic relative to the fundamental frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

FIG. 1 is a schematic perspective view of an exemplary multiple stationary coil arrangement in a commercial reactive ion etching reactor,

FIGS. 2A and 2B show cross sections of the arrangement of FIG. 1 at section 2—2 thereof and magnetic fields produced thereby at two slightly separated times during conventional operation,

FIG. 2C shows current waveforms for producing the magnetic fields shown in FIGS. 2A and 2B,

FIGS. 3A and 3B show cross-sections of the arrangement of FIG. 1 at section 2—2 thereof and magnetic fields produced thereby at two slightly separated times during operation in accordance with the invention, and

FIGS. 4A and 4B show waveforms used in accordance with the invention for respective variations of operation of the invention,

FIG. 4C shows a cross-section of the arrangement of FIG. 1 and illustrates the magnetic field produced by the waveform of FIG. 4

FIGS. 5A and 5B show further variant waveforms useful in the practice of the invention, and

FIG. 6 shows a cross-section of the arrangement of FIG. 1 at section 2—2 thereof and magnetic fields produced thereby in accordance with the waveforms of FIG. 5B

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Referring now to the drawings, and more particularly to FIG. 1, there is shown in perspective view the coil arrangement of an exemplary reactive ion etching (RIE) reactor vessel or chamber **15**, shown in plan view in FIGS. **2A**, **2B**, **3A**, **3B**, **4C** and **6**. It is to be understood that while the invention will be described below in regard to a reactive ion etching process, plasmas are also employed in many other processes which may be involved in the manufacture of semiconductor electronic devices such as plasma enhanced chemical vapor deposition (PECVD). Since the behaviors of charged particles in electric and magnetic fields are independent of the purpose for which the plasma is developed, the invention is applicable to the control of plasmas used in processes and apparatus other than for reactive ion etching in which uniformity of plasma density and potential are of importance.

It is also to be understood that while the coil geometry illustrated in FIG. 1 represents tools now in use, no admission is made that any portion of FIG. 1 is prior art in regard to the present invention. In particular, the magnetic fields and motion thereof producible by such geometry is dependent on the electrical currents in the coils (e.g. electromagnets) and the manner in which the coils are connected to current drivers (e.g. **90** of FIG. 3B) which are not depicted in FIG. 1 and, as will be discussed below, the invention differs significantly from known techniques of driving the arrangement of FIG. 1.

Specifically, the arrangement of FIG. 1 includes four generally rectangular coils **10**, **20**, **30**, **40** located with axes on or parallel to (e.g. above) orthogonal diameters of wafer **50**. Conventionally these coils are connected in pairs (generally in series so that currents in each coil of a pair will be identical to each other) having a common axis. Thus, when a pair of coils is energized, as illustrated in FIG. 2A, a relatively uniform Helmholtz magnetic field **16** is developed across wafer **50**. (In FIGS. 2A, 2B, 3A, 3B and 6, which are all taken along section line 2—2 of FIG. 1, current in respective vertical legs 11*a*, 11*b*, 12*a*, 12*b*, 13*a*, 13*b*, 14*a* and 14*b* of coils **10**, **20**, **30** and **40**, respectively, is illustrated by the convention of a cross indicating a current into the plane of the page and a circle indicating a current out of the plane of the page.)

Since an electric field E (FIG. 1) is produced toward the wafer (into the page in the top section shown in FIG. 2A along the section lines 2—2 shown in FIG. 1) by the rectification effect of the plasma and capacitance of the RF power source, energetic electrons will drift in a direction perpendicular to both the electric field and the magnetic field. This effect is thus referred to as a ExB drift. The ExB drift will be in the direction shown, resulting in further ionization of the plasma and a gradient of plasma density and plasma potential across the wafer, as alluded to above.

When both pairs of coils are energized (but at a reduced current if sinusoidally varying currents separated in phase by 90° are used, as is conventional and illustrated in FIG. 2C), a similar, substantially uniform magnetic field is produced across the wafer which is rotated 45° counter-clockwise from that of FIG. 2A as shown in FIG. 2B. (It should be noted from FIG. 2C that currents 1 and 3 and 2 and 4 are inverted with respect to each other. Conventionally therefore, these inversions are achieved by connection of the respective coils of a pair and only two current drivers are used. Four waveforms are illustrated in FIG. 2C to observe identical connection conventions for all four coils in order to facilitate comparison with waveforms utilized in the practice of the invention.) The ExB drift direction is similarly rotated in the same direction and by the same amount so that further ionization will occur and cause the gradient of plasma density and plasma potential which may cause damage on the wafer as alluded to above.

However, if the coils are not driven in pairs and adjacent coils are energized as shown in FIG. **3B**, the magnetic field **16'** is substantially changed and a gradient of magnetic field strength or intensity is developed such that magnetic field strength decreases in the direction of ExB drift. It will be recognized that the energization illustrated in FIG. **3B** is the same as that for coil legs **11***a*, **11***b* **12***a* and **12***b* of FIG. **2A** but with no current in the other two coils. Thus, with only two adjacent coils energized which are asymmetrically arranged within the reactor and relative to the wafer location, a gradient of magnetic field strength will be produced across the wafer in which the magnetic field strength decreases in the direction of ExB drift. Thus drift of energetic electrons and further ionization will be compensated by reduced confinement of the plasma in the direction of ExB drift and plasma density and potential will become more uniform across the wafer.

It should be appreciated that the presence of the average magnetic field continues to confine the plasma allowing reduction of bias while the non-uniformity of the magnetic field increases the uniformity of the density and potential of the plasma entirely independently of rotation of the magnetic field. The fact that uniformity of the plasma density is increased independently of magnetic field rotation is important to determining the magnetic field gradient and harmonic content to be optimum for the parameters of a particular RIE process, as will be discussed below.

It should be noted that FIG. **3A** corresponds to FIG. **2A** which produces a uniform magnetic field. If the energization pattern of FIG. **3B** follows that of FIG. **3A**, the magnetic field will rotate in the same manner as described above in regard to FIGS. **2A** and **2B** and will also vary between states of being substantially uniform, during which time a gradient of plasma density and potential will develop, and having a gradient of magnetic field strength decreasing in the direction of ExB drift, during which time the plasma density and potential will tend to become more uniform. While this is not the preferred method of operation of the invention, it should be noted that operation in the energization sequence illustrated in FIGS. **3A** and **3B** will cause the gradient of plasma density and potential to fluctuate and, on average, to be reduced.

Such a mode of operation could potentially provide overall increase of uniformity of average plasma exposure in some cases but since ionization due to ExB drift develops very rapidly (milliseconds or fractions of milliseconds) relative to the maximum speed of field rotation (about one-half second per cycle due to the large inductance, eddy currents and the like which are presented by large coils and yokes and conductivity of the reactor vessel **15** in RIE tools) the ability to increase RF power and tool throughput without wafer damage would not be optimally achieved. By the same token, it should be understood that FIG. **3A** is also fairly representative of a relatively uniform magnetic field which would transiently occur as the energization pattern of FIG. **3B** is switched from corner to corner to rotate the magnetic field, as will be described below, due to the same inductances and eddy currents which limit speed of field rotation. However, in this latter case, the magnetic field is somewhat less uniform during switching and maximum magnetic field uniformity occurs so transiently that RF power can be increased significantly and throughput of the reactor can be substantially increased without wafer damage.

In the preferred mode of operation, the essential feature of the driving current waveforms to develop a non-uniform magnetic field **16'** which decreases in strength in the direction of ExB electron drift is to drive adjacent coils with opposite currents in sequence at each corner of the reactor. That is, with reference to FIG. **3B**, when adjacent pairs of coils **10** and **20**, **20** and **30**, **30** and **40**, **40** and **10** are driven in sequence with opposite currents, the non-uniform magnetic field pattern **16'** illustrated in FIG. **3B** develops a plasma of improved uniformity of density and potential across the wafer and, additionally, the magnetic field can be made to rotate around the chamber to sweep the plasma across the wafer surface to further improve uniformity of average exposure to the plasma by averaging exposure of the wafer to any variations in plasma density which remain.

Further, referring briefly back to FIGS. **2A** and **2B** and recalling that the use of sinusoidally varying currents result in a substantially constant and uniform magnetic field, increasing the harmonic content will also beneficially increase magnetic field non-uniformity in a repeated time-varying manner as the non-uniform field of FIG. **3B** is swept around the chamber and will thus increase both plasma density and uniformity of plasma potential to which the wafer **50** is exposed. That is, increased harmonic content as shown in FIGS. **4B**, **5A** and **5B** will cause a beneficial increase in magnetic field non-uniformity during each phase of magnetic field rotation and further, will effectively cause a faster field rotation to be superimposed on magnetic field rotation at the fundamental frequency. Thus increased harmonic content shown in the waveforms of FIGS. **4B**, **5A** or **5B** develops a combined non-uniformity of magnetic field which further increases uniformity of average wafer exposure to plasma density and potential.

In any event, some increase of harmonic content in addition to the fundamental magnetic field rotation frequency is preferred and must be provided to obtain asymmetric energization of coils in the manner discussed above in regard to FIG. **3B**. The number and magnitude of the included harmonics can be readily modified by filtering, digital waveform generation (e.g. a function generator **70** of FIG. **3B**) or other techniques which will be apparent to those skilled in the art in view of this description of the invention.

Thus, an extreme case of the preferred mode of operation of the invention is illustrated in FIG. **4A** in which a square wave where the current is zero on alternate cycles is applied to each coil with a phase offset of 90° (achieved with delays **80** or a plurality of waveform generators schematically indicated at **71**), corresponding to the four coils shown, between each pair of adjacent coils. That is, when current **1** is applied to coil **10**, current **2** is applied to coil **20**, current **3** is applied to coil **30** and current **4** is applied to coil **40**, during period **110**, the currents and magnetic fields are as shown in FIG. **3B**, linking coils **10** and **20**. Similarly, during period **120**, the shape of the magnetic field will be of the same shape but will link coils **20** and **30**, during period **130** the magnetic field will again be of the same shape but will link coils **30** and **40** and during period **140**, the magnetic field **16'** will still remain the same shape but will link coils **40** and **10**. A different phase offset would, of course, be used for a greater or lesser number of coils.

In this manner, the non-uniform magnetic field **16'** can be made to rotate about the center of the coils and across the wafer. The field strength will also fluctuate during each of periods **110**, **120**, **130** and **140** due to the inductance of the coils and harmonic content of the driving current and will, in a repeatable manner, increase average uniformity of plasma density across the wafer.

In this latter regard, it should be understood that the current waveforms of FIG. **4A** are an extreme and idealized case of the preferred operation of the invention with maxi-

mum harmonic content which may not be required for maximum uniformity of average plasma exposure across the wafer and may be difficult to achieve in view of the large eddy currents produced by the coils **10**–**40** and the conductive chamber. Reducing the rise and fall slew rates of the current drivers **90** as shown at **150** of FIG. **4***A* also reduces harmonic content and it is expected that the practice of the invention will be optimized by regulation of the harmonic content of the applied waveforms.

As indicated above, the invention provides for improved uniformity of plasma density independently of magnetic field rotation and harmonic content can be optimized and the etching tool calibrated by interpolation among results of a small number of etching (or other) processes performed without magnetic field rotation followed by inspection to determine resulting plasma exposure uniformity. Alternatively, the invention can be practiced to advantage if the net current in adjacent legs (e.g. **12***a* and **11***b*) of adjacent coils is about or more than 1.5 times the net current in any two adjacent legs of any other two adjacent coils to assure a sufficient degree of asymmetry to establish a gradient of magnetic field strength above the area where etching or other plasma process is to be performed. For example, the waveforms of FIG. **4** would provide a net current in adjacent legs of adjacent coils which is twice the net current in any other adjacent legs of any other adjacent coils.

As a perfecting feature of the invention (which can also be considered as an adjustment of the harmonic content of the driving waveforms) all four coils (or more if provided) can be simultaneously driven. That is, the current in some coils need not be zero when other coils are driven. It is only necessary to the successful practice of the invention that the driving of the coils develop a magnetic field with sufficient asymmetry to cause a gradient of magnetic field strength which decreases in the direction of ExB drift to reduce further ionization.

More specifically, the current waveforms shown in FIG. **4B** (and FIG. **5***A*, as will be described below) provide for fully driving two adjacent coils while driving remaining coils with a lower current. It should be noted, as shown in FIG. **4***C*, that all four coils are driven in the same sense as that shown in FIG. **2***B*; the reduced current in the legs of respective coils being depicted by dashed crosses and circles therein. This waveform approximates the waveform which would result from limiting the harmonic content of the energizing current to the second and fourth harmonics in addition to the fundamental and at the same amplitude. The amplitude of the lower current level should be chosen such that the net current in adjacent vertical legs of two adjacent coils approximates or exceeds 1.5 times the net current in adjacent vertical legs of any other pair of coils, as alluded to above. As illustrated in FIG. **4***C*, the resulting magnetic field remains asymmetric although to a lesser degree than shown in FIG. **3***B* and a correspondingly reduced gradient of the magnetic field decreasing in magnetic field strength in the direction of ExB drift is illustrated by the increasing spacing of field lines across the wafer.

Therefore, further ionization due to ExB electron drift in this variation of the invention will be reduced but to a lesser degree than in the embodiment of FIG. **3B** but may provide good uniformity in some processes and tools for which the embodiment of FIGS. **3B** and **4A** would be used. Depending on parameters such as wafer and or chamber size, average magnetic field, electron density and collision frequency, the amount of current drive in the opposed coils can be adjusted as described above to derive the best instantaneous plasma uniformity. In this regard and as a further perfecting feature of the invention, the applied RF power applied to form the plasma may be modulated either in graded or discrete regions of the wafer or throughout the reactor in synchronism with alteration of magnetic field strength, as indicated at **100** of FIG. **3B** to make wafer bias more uniform as current is shifted from one pair of coil legs to the next. That is, when the magnetic field is decreased during switching of the energization waveforms, the RF power is decreased to maintain constant wafer bias potential since wafer bias will tend to increase when the magnetic field decreases.

For some plasma process parameters and tools, it may be desired to increase the magnetic field gradient beyond that available from the waveforms of FIG. **4A** as discussed above. To increase the gradient, the waveforms of FIG. **4B** can be modified to effectively reverse the sense of the lower level driving current in the variation of FIGS. **4B** and **4C**, as shown in FIGS. **5B** and **6**.

In this case (which corresponds to an increase in harmonic content), the magnetic field **16**" can be reduced to zero and even reversed at a location within the chamber **15** and potentially above the wafer although it is considered preferably to limit the location of field reversal to locations beyond the edge of the wafer. Such an arrangement provides for dispersal of the ExB drift as indicated by arrows ExB' which further reduces ionization due to energetic electrons to an even greater degree than in other variations of the invention described above. RF power is reduced in order to make the wafer bias more uniform as the magnetic field changes. RF power modulation is particularly desirable when the currents reduce the magnetic field confining the plasma to zero at a location above the wafer.

In view of the foregoing, it is seen that the invention, by providing for an asymmetrical magnetic field with a gradient of field strength decreasing in the direction of ExB electron drift provides numerous techniques for optimizing uniformity of plasma density, plasma potential and wafer bias for particular plasma process parameters such as particular gases and pressures in a manner which is independent of magnetic field rotation. This allows RF power to be increased and or modulated in synchronism with variation of magnetic field strength to further increase uniformity of wafer bias and tool throughput without damage to the wafer or delicate structures thereon. Further, for a given RF power, bias and pressure, the invention provides increased efficiency of tool operation since plasma density can be maximized over a greater area.

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced with modification, such as including more or fewer coils symmetrically arranged around the wafer or a plurality of wafers, within the spirit and scope of the appended claims.

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. A method of manufacturing including the steps of

forming a plasma including electrons and charged species,

applying an electric field across the plasma, and

confining the plasma with a variable magnetic field having a gradient of field strength which decreases in the direction of drift of electrons in response to said electric field and said magnetic field and wherein said magnetic field is developed in response to currents in a plurality of coils.

2. A method as recited in claim 1, including the further step of

rotating said magnetic field.

3. A method as recited in claim 1, wherein said currents and said magnetic field vary at a fundamental frequency and a harmonic of said fundamental frequency.

4. A method as recited in claim 3, including the further step of

modulating said RF power in synchronism with variation of said magnetic field.

5. A method as recited in claim 1, wherein said currents are square waves with zero current during alternating cycles.

6. A method as recited in claim 1, wherein the number of coils in said plurality of coils is four.

7. Apparatus for plasma processing of a material, said apparatus including

a source of RF power to produce a plasma,

at least three electromagnets including respective current drivers therefor, and

a function generator means for producing a waveform including a fundamental frequency and at least one harmonic of said fundamental frequency, and

means for providing said waveform to respective ones of said current drivers at respective times to produce a rotating magnetic field, said magnetic field being asymmetric and decreasing in intensity in the direction of ExB drift of electrons in said plasma.

8. Apparatus as recited in claim 7, including a function generator means for each of said electromagnets.

9. Apparatus as recited in claim 7, wherein said means for providing said waveform to respective ones of said current drivers includes

delay means for providing a delay of said waveform to at least two of said respective current drivers.

10. Apparatus as recited in claim 7, including four electromagnets.

11. Apparatus as recited in claim 7, including means for modulating said RF power in synchronism with application of said waveform to respective ones of said current drivers.

12. A method of operating a plasma processing device having a plurality of electromagnets and a source of RF power to provide a plasma, said method including the steps of

energizing said plurality of electromagnets asymmetrically to produce a magnetic field having a gradient of magnetic field intensity decreasing in a direction of ExB electron drift with a waveform including a fundamental frequency and at least one harmonic of said fundamental frequency, and

adjusting relative magnitude of said harmonic relative to said fundamental frequency.

13. A method as recited in claim 12, including the further step of

adjusting the number of harmonics utilized in said energizing step.

14. A method as recited in claim 12, including the further step of

energizing said plurality of electromagnets in timed sequence with said waveform to rotate.

15. A method as recited in claim 13, including the further step of

energizing said plurality of electromagnets in timed sequence with said waveform to rotate.

16. A method as recited in claim 12, including the further step of

introducing an etchant into said plasma processing device.

17. A method as recited in claim 14, including the further step of

introducing an etchant into said plasma processing device.

18. A method as recited in claim 15, including the further step of

introducing an etchant into said plasma processing device.

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